REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 22, 24, 49, 64 and 66 have been amended. No new matter has been added. Claims 1-67 remain pending. The remarks below refer to the claims as amended herein.

Amendments to the Specification

Applicant has amended the specification to correct a typographical error on page 10. No new matter has been added.

Previously-Filed Drawing Amendment

Applicant amended Figures 5 and 18 of the drawing in a Preliminary Amendment filed February 13, 2004, but has not received an acknowledgement that the Preliminary Amendment has been entered. Applicant respectfully requests that the Preliminary Amendment be entered and that an acknowledgement of entry be communicated to applicant. If a copy of the Preliminary Amendment is required, the Examiner is requested to contact the undersigned attorney.

Claim Rejections – 35 U.S.C. § 112

Claim 21 has been rejected under 35 U.S.C. § 112 as lacking clear antecedent basis for the expressions "the second circuit" and "the first circuit." Applicant has amended claim 21 to depend from claim 23 and respectfully submits that the reason for rejection is overcome. No new matter has been added.

Claim Rejections – 35 U.S.C. § 102

Claims 21-26, 41-45 and 57-63 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,796,758 to Levitan ("Levitan"). Applicant respectfully disagrees with this reason for rejection.

As to claim 21, applicant submits that Levitan does not disclose or suggest the following limitation:

> an error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells.

Levitan discloses CAM cells arranged in rows and columns with the CAM cells in each

row being coupled together by a word line and a match line (Levitan, col. 2, line 66 - col. 3, line 3). The word lines are coupled to a parity generator formed by a cascade of exclusive OR gates (Levitan, col. 3, line 15-32; Fig. 1) so that, if more than one word line is selected by an input word (and the number of selected word lines is an even number), the parity generator will output a '1' bit to enable an error condition to be signaled (Levitan, col. 3, line 33 - col. 4, line 6). Thus, Levitan is directed to signaling an error when multiple word lines are selected. Levitan does not disclose or suggest an error detection circuit coupled to receive a data word from a selected one of the rows of CAM cells, nor does Levitan disclose that the error detection circuit is coupled to receive a corresponding validity value from one of the validity storage cells.

Accordingly, because Levitan does not disclose all the limitations of claim 21, applicant submits that Levitan does not anticipate claim 21. Because claims 22-26 depend from and further limit claim 21, applicant submits that claims 22-26 also are not anticipated by Levitan.

Applicant notes that no rationale for the section 102 rejection of claim 26 is provided in the Office Action.

As to claim 41, applicant submits that Levitan does not disclose or suggest the following limitation:

> asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word.

As discussed above, Levitan is directed to signaling an error when multiple word lines are selected. Levitan does not disclose or suggest a validity value that corresponds to a selected data word, much less "asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word."

Because Levitan does not disclose all the limitations of claim 41, applicant submits that Levitan does not anticipate claim 41. Because claims 42-45 depend from and further limit claim 41, applicant submits that claims 42-45 also are not anticipated by Levitan.

As to claim 57, applicant submits that Levitan does not disclose or suggest the following limitation:

> detecting means for detecting when a valid one of the data words has an error.

Levitan discloses signaling an error when multiple word lines are selected, but does not disclose or suggest detecting when a data word is a valid data word and therefore does disclose or suggest means for detecting when a valid one of the data words has an error, as recited in claim 57. Therefore, applicant submits Levitan does not anticipate claim 57. Because claims 58-63 depend from and further limit claim 57, applicant submits that claims 58-63 also are not anticipated by Levitan.

Claim Rejections – 35 U.S.C. § 103(a)

Claims 1-13, 16-20, 27-30, 32-40, 46-48 and 64-67 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 6,154,384 to Nataraj et al. (Nataraj) in view of Levitan. Applicant respectfully disagrees with this reason for rejection.

Claim 1 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, concurrently with the compare operation, whether the selected data word includes an error.

As discussed above in reference to claim 21, Levitan discloses a parity generator coupled to word lines of a CAM array so that, if more than one word line is selected by an input word (and the number of selected word lines is an even number), the parity generator will output a '1' bit to signal the multiple selected word line condition. Levitan does not disclose an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells. Accordingly, as Nataraj also does not disclose the above-recited limitation, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would not include all the limitations of claim 1 and therefore would not render claim 1 obvious. Because claims 2-13 depend from and further limit claim 1, claims 2-13 also are not obvious in view of a combination of Nataraj and Levitan.

Claim 16 recites in part:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from a selected one of the rows of CAM cells and a corresponding validity value, the error detection circuit including a first circuit to determine whether the selected data word includes an error, and a second circuit, responsive to an error indication from the first

circuit, to output an error signal if the selected data word is determined to include an error, the second circuit including an input to receive the validity value that corresponds to the selected data word and being adapted to prevent assertion of the error signal if the validity value indicates that the selected data word is not a valid data word.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would still lack the above-recited limitation. Accordingly, applicant submits that claim 16 is not obvious in view of a combination of Nataraj and Levitan. Because claims 17-20 depend from and further limit claim 16, applicant submits that claims 17-20 also are not obvious in view of a combination of Nataraj and Levitan.

Claim 27 recites in part:

an error detection circuit coupled to receive, via the bit lines, a data word from the selected one of the rows of CAM cells and to determine whether the data word includes an error.

Applicant submits that, at least for the reasons given with respect to claim 1, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would not include the above-recited limitation and therefore that claim 27 is not obvious in view of a combination of Nataraj and Levitan. Because claims 28-30 and 32-34 depend from and further limit claim 27, applicant submits that claims 28-30 and 32-34 also are not obvious in view of a combination of Nataraj and Levitan.

Claim 35 recites in part:

determining, concurrently with the compare operation, whether a selected one of the data words includes an error.

Levitan discloses signaling an error when multiple word lines are selected, but does not disclose or suggest determining whether a selected one of the data words includes an error. Because Nataraj also does not disclose determining whether a selected one of the data words includes an error, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would still lack the above-recited limitation of claim 35 and therefore would not render claim 35 obvious. Because claims 36-40 depend from and further

limit claim 35, claims 36-40 also are not obvious in view of a combination of Nataraj and Levitan.

Claim 46 recites, in part:

> receiving from the CAM device, an address of a storage location within the CAM device that contains a corrupted data value;

Applicant submits that neither Nataraj nor Levitan discloses the above recited limitation and therefore that, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would not include the above-recited combination. Accordingly, applicant submits that claim 46 is not obvious in view of a combination of Nataraj and Levitan. Because claims 47 and 48 depend from and further limit claim 46, applicant submits that claims 47 and 48 also are not obvious in view of a combination of Nataraj and Levitan.

Claim 64 recites, in part:

> means for concurrently (i) determining whether a data word stored in a selected row of the CAM cells has an error, and (ii) comparing comparand data with the data words.

Applicant submits that, at least for the reasons given above in reference to claim 35, neither Nataraj nor Levitan discloses the above recited limitation and therefore that, even if Nataraj and Levitan could be combined in the manner suggested in the Office Action, the combination would not include the above-recited combination. Accordingly, applicant submits that claim 64 is not obvious in view of a combination of Nataraj and Levitan. Because claims 65-67 depend from and further limit claim 64, applicant submits that claims 65-67 also are not obvious in view of a combination of Nataraj and Levitan.

Claims 14, 15 and 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nataraj and Levitan and further in view of "Error Correction with Hamming Codes," pp.1-2 downloaded June 22, 2001 from URL, http://www.rad.com/networks/1994/err-con/hamming.htm (hereinafter the "Error Correction reference").

As discussed above, neither Nataraj nor Levitan discloses the following limitation of claim 1, a limitation incorporated by dependency into claims 14 and 15:

> an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine,

concurrently with the compare operation, whether the selected data word includes an error.

Applicant submits that the Error Correction reference also does not disclose the above-recited limitation so that, even if Nataraj, Levitan and the Error Correction reference could be combined as suggested in the Office Action, the combination would still lack the above-recited limitation. Accordingly, applicant submits that claims 14 and 15 are not obvious in view of a combination of Nataraj, Levitan and the Error Correction reference.

As discussed above, neither Nataraj nor Levitan discloses the following limitation of claim 27, a limitation incorporated by dependency into claim 31:

an error detection circuit coupled to receive, via the bit lines, a data word from the selected one of the rows of CAM cells and to determine whether the data word includes an error.

Applicant submits that the Error Correction reference also does not disclose the above-recited limitation so that, even if Nataraj, Levitan and the Error Correction reference could be combined as suggested in the Office Action, the combination would still lack the above-recited limitation. Accordingly, applicant submits that claim 31 is not obvious in view of a combination of Nataraj, Levitan and the Error Correction reference.

Claims 49-56 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nataraj and Levitan and further in view of information provided in the Background section of the present application (hereinafter the "Application Background").

Claim 49 recites in part:

a CAM device coupled to the plurality of signal lines, the CAM device including an error checking circuit to automatically check each of a plurality of data values stored within the CAM device for error and to signal the processor via one or more of the plurality of signal lines in response to detecting an error in any one of the plurality of data values.

Levitan discloses signaling an error when multiple word lines are selected, but does not disclose or suggest an error checking circuit to automatically check each of a plurality of data values stored within the CAM device for error. Nataraj also does not disclose such an error checking circuit. Applicant further submits that the Application Background merely describes

using stored parity information to detect an error when a host device instructs the CAM device to perform a read operation, not an error checking circuit to automatically check each of a plurality of data values stored within the CAM device for error. Accordingly, even if Nataraj, Levitan and applicant's Background could be combined in as suggested in the Office Action, the combination would still lack the above-recited limitation of claim 49 and therefore would not render claim 49 obvious. Because claims 50-56 depend from and further limit claim 49, applicant submits that claims 50-56 also are not obvious in view of a combination of Nataraj, Levitan and the Application Background.

Conclusion

Applicant respectfully submits that claims 1-67 are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

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